REMARKS

SUMMARY:

Claims 6, 7, 10, and 12 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,215,372 (Novak). Claims 8, 9, 11, and 13 stand rejected under 35 U.S.C. §103(a) as unpatentable as being obvious solely over Novak.

Responses to the characterizations summarized above and traversal of the stated prior art rejection grounds are respectfully hereafter presented with respect to each individual aspect of the Office Action.

BACKGROUND CASE LAW RE 35 U.S.C. §102 & §103:

Before setting forth a discussion of the rejection grounds applied in the most recent non-Final Office Action, it is respectfully submitted that controlling case law has frequently addressed rejections under Sections 102 and Section 103.

"For a prior art reference to anticipate in terms of 35 U.S.C Section 102, every element of the claimed invention must be identically shown in a single reference." Diversitech Corp. v. Century Steps, Inc., 850 F.2d 675, 677, 7 U.S.P.Q.2d 1315, 1317 (Fed Cir, 1988; emphasis added). The disclosed elements must be arranged as in the claim under review. See Lindemann Machinefabrik v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). If any claim, element, or step is absent from the reference that is being relied upon, there is no anticipation. Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565, 230 U.S.P.Q. 81 (Fed. Cir. 1986). Anticipation under 35 U.S.C. Section 102 requires that there be an identity of invention. See Shatterproof Glass Corp. v. Libbey-Owens Ford Co., 758 F.2d 613, 225 U.S.P.Q. 635, 637 (Fed. Cir. 1985). In PTO proceedings, claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. In re Sneed, 710 F.2d 1544, 1548, 218 U.S.P.Q. 385, 388 (Fed. Cir. 1983).

In addition to the well-known required multi-step analysis of Graham v. John Deere Co., 381 U.S. 1, 148 U.S.P.Q. 459 (S. Ct. 1966), and its progeny, the Court of

Appeals for the Federal Circuit has on numerous occasions offered its guidance concerning the propriety of Section 103 rejections.

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so. (emphasis original)

ACS Hospital Systems, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984).

The task of the Patent Office is essentially a burden of proof not just to show prior patents with selected elements similar to respective parts of a claimed combination, but to show teachings to support obviously combining the elements in the manner claimed.

> Virtually all inventions are necessarily combinations of old elements. The notion, therefore, that combination claims can be declared invalid merely upon finding similar elements in separate prior patents would necessarily destroy virtually all patents and cannot be the law under the statute, ' 103. (footnotes omitted)

Panduit Corp. v. Dennison Manufacturing Co., 1 U.S.P.Q. 2d 1593, 1603 (Fed. Cir. 1987).

In In re Deminski, 230 U.S.P.Q. 313 (Fed. Cir. 1986), the court reversed a Patent Office Board of Appeals decision rejecting claims for obviousness, saying: "There [was] nothing in the prior art references, singly or in combination, 'to suggest the desirability, and thus the obviousness' of the [claimed subject matter]." Id. at 315; emphasis original. The court noted that the relied-on reference did not address the technical problem addressed by the claimed invention (and in fact taught away from the Applicant's invention), and stated the well-established principle that "[h]indsight analysis is clearly improper. . . ." Id. at 316.

In Bausch & Lomb v. Barnes-Hind/Hydrocurve, 230 U.S.P.Q. 416 (Fed. Cir. 1986), the court vacated a district court holding of invalidity for obviousness. In doing

so, the district court was criticized for viewing teachings from the prior art in isolation, instead of considering the prior art references in their entirety; for entering the tempting but forbidden zone of hindsight analysis; for failing to view the claimed invention as a whole; and for disregarding express claim limitations. Id. at 419, 420.

> It is impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one skilled in the art. (citations omitted)

Bausch & Lomb v. Barnes-Hind/Hydrocurve, 230 U.S.P.Q. 416, 419 (Fed. Cir. 1986). (emphasis added)

> The Supreme Court in Graham and Adams . . . foreclosed the use of substitutes for facts in determining obviousness under section 103. The legal conclusion of obviousness must be supported by facts. [footnote omitted] Where the legal conclusion is not supported by facts, it cannot stand. . . .
>
> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. . . . It [the Patent Office] may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis. . . .
>
> [W]e may not resolve doubts in favor of the Patent Office determination when there are deficiencies in the record as to the necessary factual bases supporting its legal conclusion of obviousness. (emphasis original)

In re Warner, 379 F.2d 1011, __, 154 U.S.P.Q. 173, 177, 178 (C.C.P.A. 1967).

Finally, the PTO Board of Appeals noted the following in Ex parte Clapp:

"[S]implicity and hindsight are not proper criteria for resolving the issue of obviousness. " Ex parte Clapp, 227 U.S.P.Q. 972, 973 (PTO Bd. App. 1985).

REJECTION OF ORIGINAL CLAIMS 6, 7, 10 AND 12 (35 U.S.C. §102(e)):

Original claims 6, 7, 10 and 12 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,215,372 (Novak). Based on the present subject matter of such claims, and the following remarks, Applicants respectfully traverse such alleged anticipation and respectfully request withdrawal of such rejections.

Original and currently amended claims 6, 7, 10, and 12 are directed to a method for adjusting the equivalent series resistance (ESR) of a multi-layer component. The method includes providing various layers in a multi-layer component, including a resistive layer, and then adjusting properties of the resistive layer to vary the ESR of the component.

It should be appreciated that Applicants' basic configuration as representatively illustrated in application Figure 1B is directed to a multi-layer component that corresponds to at least four separate layers of material layered successively over each other. Thus, there is a first electrically conductive layer on top of which resides an insulating or dielectric layer, on top of which further resides a resistive layer, and finally on top of which still further resides another conductive layer.

The original specification, including in lines 15-25 of page 19 thereof, sets forth one example that discusses more particular aspects of a technique as set forth in claims 6, 7, 10, and 12. With reference to Fig. 1B of the subject application, an insulating (dielectric) layer 22 and resistive barrier layer 34 are provided between a bottom electrode 20 and a top electrode 24 (which are respective conductive layers).

Respective arrays of circular openings are provided in the top electrode layer 24 and in the resistive layer 34. By forming the circular openings in electrode layer 24 larger than the respective openings in resistive layer 34, additional portions of resistive layer 34 are exposed. Relative more exposure of the resistive layer 34 increases the ESR of the multilayer component.

Selection of such exposure area can in accordance with the present subject matter serve to "tune" the ESR of the multilayer component, making it possible to design

and provide a component that reduces, for example, potential ringing in a resultant circuit application.

Significantly, from a manufacturing standpoint, it is possible to manufacture a basic component and then "tune" the component to accommodate specific buyer requirements. In such manner, a manufacturer may stockpile basic product while awaiting specific final specifications from one or more buyers.

The recent Office Action asserts that Novak discloses all elements of independent claim 6, including providing various electrically conductive layers, insulating layers, and a resistive layer as well as adjusting ESR of the component. Such overall position of the USPTO is respectfully traversed, inasmuch as there are several differences between the subject matter disclosed in Novak and the subject claimed methods. The Office Action states in pertinent part (on numbered pages 2 and 3 thereof)(emphasis original):

> **With regard to claim 6,** Novak teaches a method for reducing electrical resonances and noise propagation in multilayer board, comprising:
>
> - producing a multilayer component (Fig. 6, 600) including at least first and second electrically conductive layers (Fig. 6, items 602 and 606) separated by an insulating layer (Fig. 6, items 610);
>
> - providing a resistive layer (Fig. 6, 650 or 652); lines 9-12) with the insulating layer and the first and second electrically conductive layers; and
> - adjusting the ESR (Col. 8, lines 59-61; col. 9, lines 5-20) of the component by varying the effective resistance of the resistive layer.

Applicants respectfully note that the above-recited positions of the Office Action with reference to claim 6 **improperly omit a claimed feature**.

More specifically, claim 6 (as presently amended as well as all its prior versions), clearly calls for "... a resistive layer ***layered with*** the insulating layer ..." Applicants respectfully urge that the incorporation of slugs of material as at 650, 652 of Novak to produce ***capacitive islands*** within insulating layer 612 can **not** be properly construed

as corresponding to "a resistive layer ... ***layered with*** the insulating layer" as presently (and as previously) recited.

At most, the Novak slugs of material 650, 652 correspond to resistive areas combined with or mixed with a layer of insulating material, not "layered with ... the insulating layer" as claimed.

Without entry of any new matter, Applicants have amended the language of independent method claim 6 to include "providing a resistive layer layered with and substantially covering the insulating layer" as an approach and effort to further clarify the above-noted distinction, without intending to otherwise affect the scope of the present subject matter.

The recent Office Action asserts in pertinent part (top of numbered page 7) that "... Novak teaches that the dielectric islands can have its adjusting resistance by suspending conductive particles within its binder material ...." Applicants recognize generally that varying portions of conductive material will provide adjustability of resistance. However, Applicants strongly disagree that the structure disclosed by Novak, when properly considered, renders obvious the specific methodology as presently claimed.

In contrast, Novak is concerned with a multilayer substrate or circuit board, which is an element on which integrated circuits are often built. Such generally is a different technology from multi-layer components, which in contrast is the focus of the presently claimed subject matter. The importance of such basic distinction between circuit substrates versus multi-layer components should be better appreciated from the following additional discussion of the Novak reference and the present claims.

More specifically, per Novak's disclosure, his primary concern is directed to the reduction of electrical resonance and noise propagation in a multi-layer circuit board construction using planar power and ground planar conductors. Novak proposes that in order to achieve his objective he divide his multi-layer circuit board into an effective grid arrangement by providing uniformly spaced islands of material having dielectric constants higher than the dielectric constants of the surrounding insulator. An example of Novak's grid-like equivalent structure is shown in his Figure 2.

Applicants strongly urge that such disclosure relative to multi-layer printed circuit boards having power planes included therein is far removed from the component and method taught and claimed by Applicants.

Further, Applicants suggest that Novak's disclosure is so far removed from the presently claimed subject matter that those of ordinary skill in the art would not be motivated at all to employ such disclosed techniques to provide equivalent series resistance adjustment for an electrical component, as presently claimed.

Just as one example of practical considerations arising due to such basic distinction, there are several orders of magnitude differences in sizes between the two technologies. For example, Novak column 2, lines 41-49 describe the FR4 circuit as being on the order of 10 inches on a side. While the present application does not focus on the subject of size per se, those of ordinary skill in the art would appreciate that present components would be more on the order of 0.1 inches. Likewise, the Novak part would, for example, consist of relatively thick copper (about 1.4 mils per the above specification reference to Novak) and FR4, about 2 mils, while the present subject matter would more typically use silicon substrates, and have features measured in microns.

Still further, in the Novak part, the resistive elements are in essence "buried" in the board, within "capacitive islands", well away from the components, while in the present subject matter, resistors are intimate with effective connections.

The subject Office Action literally equates capacitive islands 650 and 652 of Novak with the resistive layer subject matter set forth in claim 6 by stating: "providing a resistive layer (Fig. 6, 650 or 652; col. 9, lines 6-12)."

It is respectfully not accurate to characterize capacitive ***islands*** 650 or 652 as a "resistive layer". A layer, as defined in Webster's New Collegiate Dictionary, Ninth Edition, is "one thickness, course, or fold laid or lying over or under another." This definition is representative of the ordinary meaning of the term layer. As layers are generally understood and as also described in both the subject application and in the Novak patent, capacitive ***islands*** 650 and 652 are not separate **layers**, but an integral portion of another layer.

Likewise, the Office Action position should not view such **capacitive** islands 650 and 652 as the same as the **resistive** layers of the present subject matter, and there is no adequate justification for doing so.

To persist in either of such above-referenced positions is to respectfully fall prey to the improper practice of hindsight application of references.

Based on the above distinctions, Applicants respectfully submit that the capacitive islands in Novak do not correspond to a "resistive layer" separate from electrically conductive layers and an insulating layer. Therefore, as a matter of law, Novak can not anticipate the pertinent claimed subject matter.

Currently presented claim 6 sets forth the steps of producing a multilayer component including at least first and second electrically conductive layers separated by an insulating layer, and providing a resistive layer layered with and substantially covering the insulating layer and the first and second electrically conductive layers. The subject Office Action equates planar conductors 602, 604, 606 or 608 of Novak with the electrically conductive layers of claim 6, and layers 610, 612 or 614 with the insulating layer of claim 6.

The recent Office Action in the middle of numbered page 7 thereof notes in pertinent part that: "... it appears that applicants try to miscompare the prior art Novak and the said claimed invention..." and invites Applicants "... to revisit the claimed rejection as stated in section 3 above." Applicants have revisited both the rejection and their previous statement, and respectfully conclude that misapplication of Novak to the claimed invention is a more appropriate conclusion.

The entire disclosure with respect to any specifics of Fig. 6 of Novak can be found at column 7, starting with line 15 thereof and stating in total:

> FIG. 6 is a cross-sectional view of a portion of a multi-layer electronic substrate 600 which corresponds to the structure illustrated in FIG. 4, but incorporates capacitive islands in accordance with the first inventive embodiment. Elements in FIG. 6 which correspond to elements in FIG. 4 have been given corresponding numeral designations. For example, in the substrate illustrated in FIG. 6, there are four planar electrical conductors: a first signal planar conductor 602, a

ground planar conductor 604, a power planar conductor 606, and a second signal planar conductor 608. These conductors correspond to the four planar conductors 402, 404, 406 and 408 illustrated in FIG. 4. FIG. 6 also illustrates the capacitive islands 650 and 652 which are spaced at a distance s and capacitively load the power and ground planar conductors 604 and 606.

It should be immediately noticed that reference characters 610, 612, and 614 pointed to by the Examiner do not appear anywhere in Novak's specification. This fact can easily be confirmed by text search of the document. If one **assumes** that layers 610, 612 or 614 are dielectric layers based on the actual disclosure in Novak quoted herein immediately above, then such layers still do **not** correspond to the insulating layer subject matter claimed in claim 6.

In fact, if one for some reason perceives for example that layer 612 is "analogous" to layer 412, it is noted that layer 412 is instead variously referred to as "a second dielectric layer 412" (Novak, Col. 5, line 65), a "first signal planar conductor 412" (Novak, Col. 6, line 7), the "insulating layer 412" (Novak, Col. 6, line 37), and "the core laminate 412" (Novak, Col. 6, lines 46-47).

Based on the above distinctions, Applicants respectfully submit that Novak fails to disclose all elements of independent claim 6, especially the provision of a distinct resistive layer among the first and second electrically conductive layers and insulating layer, as well as the step of adjusting the ESR of the component by varying the effective resistance of the resistive layer. As such, Novak as a matter of law can not anticipate present independent claim 6, and such present claim 6 should be found as patentable over the Novak reference.

Since claims 7, 10, and 12 further depend from claim 6, which should otherwise be allowable per the foregoing, and further limit same, claims 7, 10, and 12 should also be allowable over Novak, and Applicants respectfully request acknowledgement of same.

Concerning dependent claim 7, notwithstanding the foregoing, Applicants further note that the capacitive islands 650, 652 of Novak (which are equated per the Office

Action with a resistive layer) are not provided "between the insulating layer and one of the first or second electrically conductive layers", as set forth in such claim 7. The Novak capacitive islands 650, 652, which are an integrated part of insulating layer 612, are provided between conductive layers 604 and 606, not inbetween an insulating layer and a conductive layer.

With reference to dependent claims 10 and 12, the subject Office Action states in pertinent part:

> **With regard to claims 10 and 12,** Novak teaches that the adjusting step comprises:
> - varying the effective resistance of the resistive layer by adjusting the composition of the resistive layer (Col. 9, lines 5-20).

However, the cited discussion of Novak does not relate to adjustments of a resistive layer, but instead adjustments to a high dielectric island. Therefore, such subject matter as a matter of law should not be regarded as anticipating the presently claimed subject matter.

Based on the foregoing, Applicants respectfully traverse the rejection of claims 6, 7, 10 and 12 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,215,372 (Novak).

REJECTION OF CLAIMS 8, 9, 11 and 13 (35 U.S.C. §103(a)):

Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Novak. Specifically, the subject Office Action states in pertinent part (on numbered pages 3 and 4 thereof)(emphasis original):

> **With regard to claim 8,** Novak teaches a method for reducing electrical resonances and noise propagation in multilayer board, including the adjusting steps of:
>
> - perforating one of the first or second electrically conductive layers (Fig. 6, items 602 or 606; Fig. 10, items 1002 or 1006) with a plurality of through-holes (Fig. 6, 622; Fig. 10, 1022); and
> - varying the effective resistance of the resistive layer by adjusting capacitive and resistive islands (Fig. 6, 652 or Fig. 10, 1052; col. 9, lines 6-29) at selected areas or

distances (Fig. 6, See Below; col. 9, lines 37-49) from vias (Fig. 6, 622 or Fig. 10,10220) whereby the extent of coverage of the perforated electrode varies the effective resistance of the resistive layer, except for detailing these selected areas or distances as varying and spacing diameters of through-holes.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to consider these selected areas or distances as varying and spacing diameters (Fig. 6, See Below; col. 9, lines 37-49) of through-holes, which can vary to adjust the resistance/capacitance and to match the impedance of the multilayer circuit in order to reduce noise and any ground bounce signal in the whole printed circuit board.

As previously described, the subject application discloses forming circular openings in one of the electrically conductive layers larger than the respective openings in an adjacent resistive layer, thereby exposing relatively additional portions of the resistive layer and relatively increasing the ESR of the multi-layer component. Such intentional selection of the amount of coverage of the perforated conductive layer relative to the adjacent resistive layer is in such exemplary embodiments what enables the "tuning" or selection of a desired ESR value.

The Examiner admits that the above features are not disclosed in Novak. Further, it is respectfully submitted they are not simply "obvious" features, as the Examiner alleges. Per pertinent case law, every element of the claims must be disclosed in a reference or combination of references.

Every element of claim 8, especially the step of adjusting the diameter of through-holes of an ***electrically conductive layer*** relative to a resistive layer, is **not** disclosed in Novak. The Office Action does **not** point to any place in Novak or another reference that discusses this feature. The Office Action also fails to point to a specific disclosure in Novak that purportedly provides any **suggestion or motivation** for "obviously" modifying the technology of Novak in a way as set forth in original claim 8.

In particular, what the Office Action refers to as the so-called "through-holes (Fig. 10, 1022)" are actually power vias which surround a high dielectric constant island 1052 and which connect to a component 1018. See Novak, col. 9, lines 45-49. In addition, placement of such power vias is a distinct consideration for Novak, relative to placement

of signal vias or placement of high dielectric constant islands. See Novak, col. 9, lines 32-45. Therefore, there is an entirely different character and purpose of the subject matter of Novak than that for which it is depended on as allegedly invalidating the present subject matter.

Furthermore, the recent Office Action asserts in pertinent part (on numbered page 4 thereof) that "it would have been obvious ... to consider these selected areas or distances as varying and spacing diameters ...." Respectfully, such statement plainly constitutes speculation of the ilk of the well known ancient rejections based on "obvious to try" criteria and are purely the product of impermissible hindsight. Such rejections are not supported by law, as amply demonstrated hereinabove.

The recent Office Action has argued in pertinent part on numbered page 7 thereof that:

> "... Novak teaches that the dielectric islands can have its adjusting resistance by suspending conductive particles within its binder material (Col. 9, lines 6-9) and separate from different layers (Fig. 6, items 602, 610, 604, 606, 614 or 608). Therefore, his islands are completely associated with the capacitance and resistance characteristics, which are critical part in matching signal impedance in order to reduce resonance in any circuit system."

Applicants respectfully submit that a disclosure to vary the "number of particles per unit volume of the particulate-binder combination" as Novak actually involves, is significantly different from the presently claimed methodology, and in no way (other than through the impermissible application of hindsight) motivates one of ordinary skill in the art to vary the effective resistance of a resistive layer "by adjusting the diameter of selected of the plurality of through-holes" as claimed in claim 8.

Applicants respectfully submit that under such circumstances, the 35 U.S.C. §103(a) rejection of original claim 8 is inappropriate, and withdrawal of such rejection is respectfully requested.

Claim 13 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Novak. Specifically, the subject Office Action states in pertinent part (numbered pages 5 and 6 thereof)(emphasis original) that:

With regard to claim 13, Novak teaches a method for reducing electrical resonances and noise propagation in multilayer board, which reads on applicants' claimed invention, including:

- producing a multilayer component (Fig. 6, 600) having a plurality of successively stacked electrode layers (Fig. 6, items 602, 604, 606 or 608);
- providing separate insulating layers (Fig. 6, items 610, 606 or 614) sandwiched between each of the electrode layer; and
- varying a physical property of selected of the separate insulating layers with different capacitance (Fig. 6, 652) whereby the resonance characteristics of the multi-layer component are adjusted (Abstract); except for having two separate insulating layers characterized by two different thicknesses, whereby the resonance characteristics of the multi-layer component are adjusted.

It is a mere matter of design choice to have two separate insulating layers characterized by two different thicknesses or more or less, whereby the resonance characteristics of the multi-layer component are adjusted, since it is known in the art that the physical property or capacitance is dependent also on the thickness (Fig. 1, h) and the dielectric constant (epsilon –r) of the insulating layer based on the mentioned equation in column 8, lines 41-44, therefore one of ordinary skill in the art, by applying the mentioned equation (Col. 5, line 10), can vary the capacitance of the conductor (Fig. 10, items 1002, 1004, 1006 or 1008) or the overall multi-layer component by varying the dielectric constant (Fig. 10, 1052; col. 7, lines 43-48) and/or the thickness of the insulating layers (Fig. 10, items 1010 or 1012 or 1014) of the substrate in order to come up with the desired capacitance for the conductor on that substrate for proper resonance. therefore varying some of the insulating layers' thickness (Fig. 10, 1010 or 1012) or the dielectric constant of the component (Fig. 10, 1052; col. 9, lines 6-9) will provide the same effect of varying the capacitance of the conductors, which results in adjusting the resonance characteristics of the multi-layer component.

Again, Applicants respectfully traverse the various views of the Office Action regarding alleged correspondence of the presently claimed subject matter and the cited portions of Novak. The Office Action seems to already recognize that there is an important deficiency of Novak relative to independent claim 13 since it notes that [all] the subject matter of claim 13 is shown "except for having two separate insulating layers characterized by two different thicknesses." However, there is respectfully no articulated basis (other than apparent hindsight) by which Novak is said by itself to bridge to the presently claimed subject matter, including the above "two different thicknesses" aspect.

With regard to independent claim 13, several additional aspects of such claim are also not disclosed in Novak. Claim 13 sets forth a step of varying the thickness of selected of the separate insulating layers in a multi-layer component. The varied thickness arrangement is such that there are insulating layers of at least two different thicknesses. Various examples of such feature set are illustrated in Figs. 6A-6E of the subject application, and include such configurations as those referred to as continuous thickness variation, patterned thickness variation, and matched variable thickness variation.

If anything, the knowledge of one of ordinary skill in the art teaches away from how one of ordinary skill in the art might "interpret" Novak vis-à-vis the present subject matter, even assuming arguendo that one of ordinary skill in the art would somehow seek to experiment with modifying Novak.

Specifically, Applicants submit that in the ordinary course of events, layers are generally preferred to be held at constant thickness, since that is the most production expedient. Changes to layers begin to introduce complex phenomena at presently higher frequencies than at which the industry presently uses various capacitance values in a single chip, particularly as one seeks to meet demands for operability at multiple frequencies. Therefore, it is generally counter-intuitive (i.e., non-obvious) to one of ordinary skill in the art to combine different thicknesses of layers, as presently claimed.

Such is all the more an important consideration when understanding that the subject matter relied on by the Office Action isn't in fact even layers, but "capacitive islands". Therefore, Novak by itself respectfully as a matter of law can not render obvious the presently claimed subject matter of independent claim 13.

Further it should be appreciated that the only disclosure in Novak relative to varying any aspect of his disclosed circuit board would appear to relate to the disclosed concept of varying the resistivity that may be incorporated into his capacitive islands by "changing the number of particles per unit volume of the particle-binder combination" as specifically recited at column 9, lines 9-10. Plainly, such disclosure would not lead one of ordinary skill in the art to conclude that resistance can be varied in plural, different layers by changing the thickness of the layers from one layer to another. Applicants

respectfully submit that such a "teaching" could only come from the use of impermissible hindsight.

Based on the foregoing, Applicants respectfully traverse the rejection of claims 8, 9, 11 and 13 under 35 U.S.C. §103(a) as unpatentable as being obvious solely in view of U.S. Patent No. 6,215,372 (Novak).

CONCLUSION:

Inasmuch as all outstanding issues have been addressed, it is respectfully submitted that the present application, including active claims 6-13, is in complete condition for issuance of a formal Notice of Allowance, and action to such effect is earnestly solicited. The Examiner is invited to telephone the undersigned at his convenience should only minor issues remain after consideration of this response in order to permit early resolution of the same.

Respectfully submitted,

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